CLAIMS

1. A graphic processing apparatus comprising:

memory means having an m-bit data bus so as to be accessed by use of a row address and a column address;

data processing means having an n-bit data bus (n > m) for delivering an address to said memory to execute a data processing; and

store means for sequentially reading out a plurality of data items having different column addresses in a row address so as to temporarily store the data items;

wherein data temporarily stored is read out from said store means so as to be delivered via the n-bit data bus to said data processing means.

2. A graphic processing apparatus comprising;

memory means having an m-bit data bus so as to be accessed by use of a row address and a column address;

data processing means having an n-bit data bus (n > m) for delivering an address to said memory to execute a data processing; and

multiplex means for multiplexing write data transferred from said data processing means so as to sequentially output resultant data onto the m-bit data bus items;

wherein data items are written at a plurality of column addresses in the row address.

3. A graphic processing apparatus comprising:

memory means having an m-bit data bus so as to be accessed by use of a row address and a column address;

data processing means having an n-bit data bus (n > m) for delivering an address to said memory to execute a data processing; and

counter means for sequentially generating a plurality of column addresses;

wherein an address supplied from said data processing means is combined with an output from said counter means so as to produce a sequential column address.

4. A graphic processing apparatus comprising:

memory means for storing therein a plurality of pixels of pixel information, each said pixel being represented by a plurality of bits, said memory means being accessed by use of a row address and a column address;

store means for sequentially reading out a plurality of data items having different column addresses in a row address so as to temporarily store the data items;

data convert means for converting the data temporarily stored into a plurality of serial signals; and

output means for outputting the serial signal obtained from said convert means.

5. A graphic processing apparatus comprising:

memory means for storing therein pixel information, said memory means being accessed by use of a row address and a column address;

store means for sequentially reading out a plurality of data items having different column addresses in a row address so as to temporarily store the data items;

data convert means for converting the data temporarily stored into a plurality of serial signals;

output means for outputting the serial signal obtained from said convert means; and

select means for selecting a number of bits constituting a pixel.

6. A graphic processing apparatus comprising:

data processing means for multiplexing an address for a memory and data so as to effect input/output operations, thereby executing a data processing; and

means for generating clock signals having alternately different periods such that a data input/output period of time is longer than an address output period of time of said data processing means.

7. A graphic processing apparatus including memory means capable of effecting read/write operations of a plurality of column data items for a row address and a controller for achieving an interface with respect to a processor conducting graphic processing,

said controller comprising:

memory control means operative in response to a control signal from said processor for indicating read/write operations of a plurality of column data items to said memory means;

first means for concatenating a plurality of data items read out from said memory means so as to produce data having a bit length which can be read by said processor;

second means for subdividing the data read out by said processor into a plurality of data items which can be written in a row address by said memory means;

means for supplying an output from said first means to said processor; and

means for delivering an output from said second means to said memory means.

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